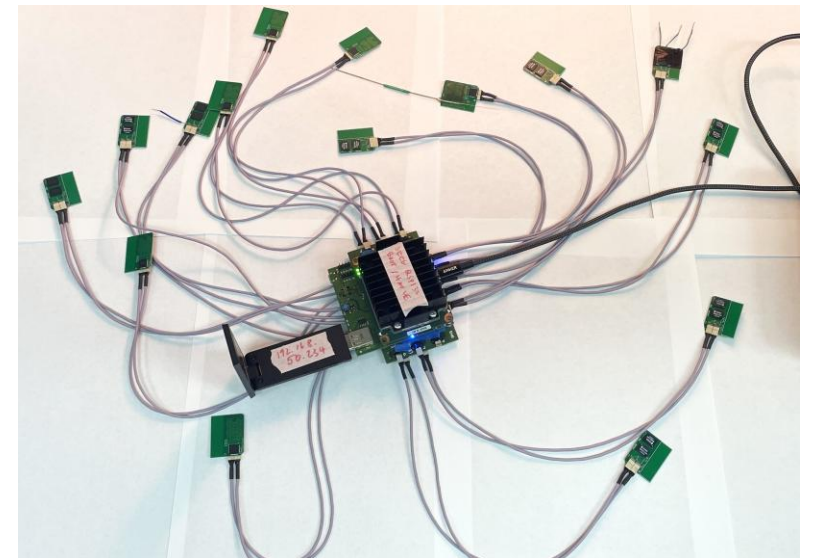
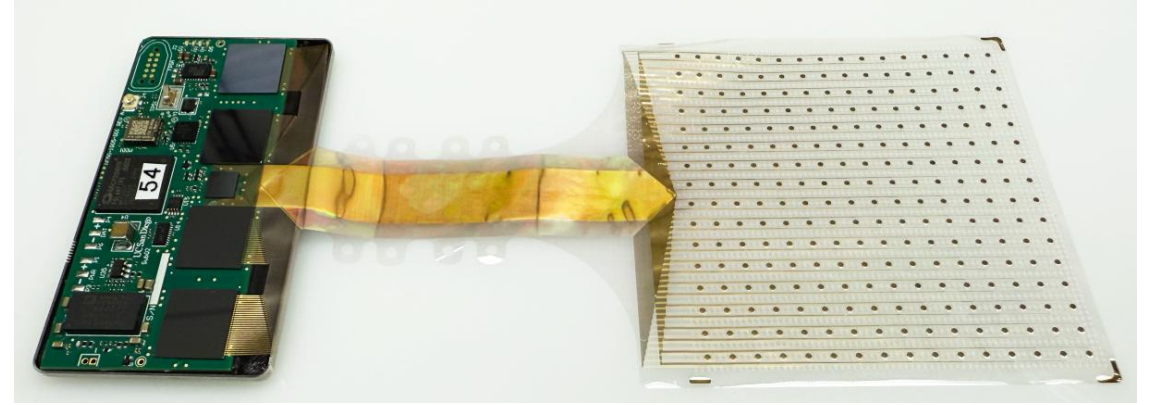
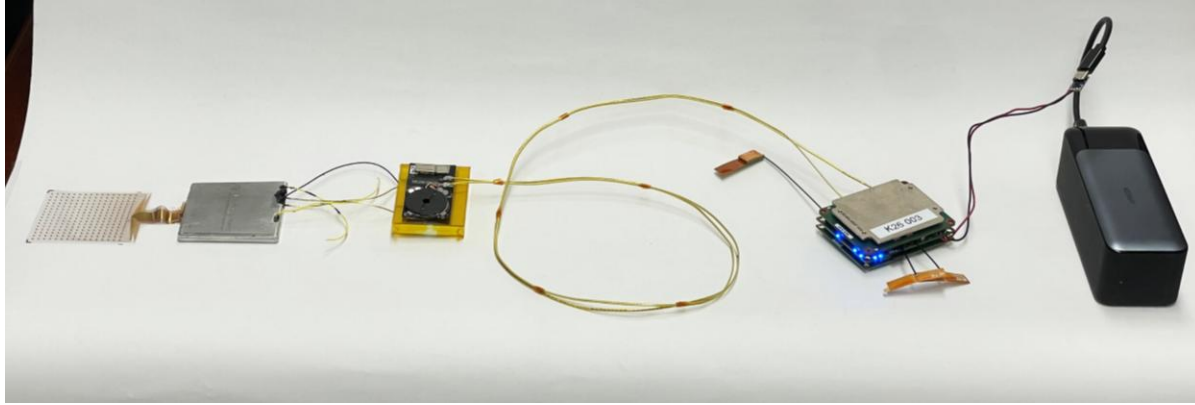


Wireless Neuromonitoring System Project

Hao Le



Hao Le

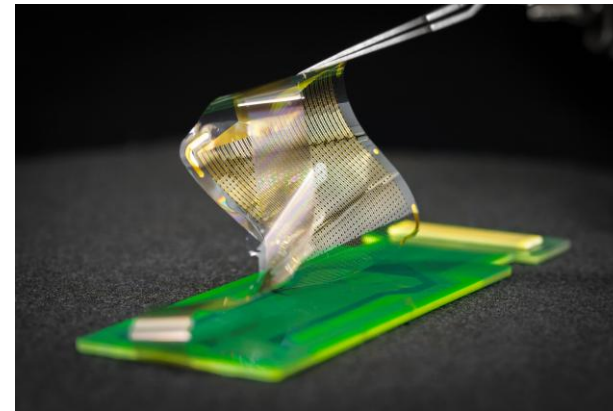
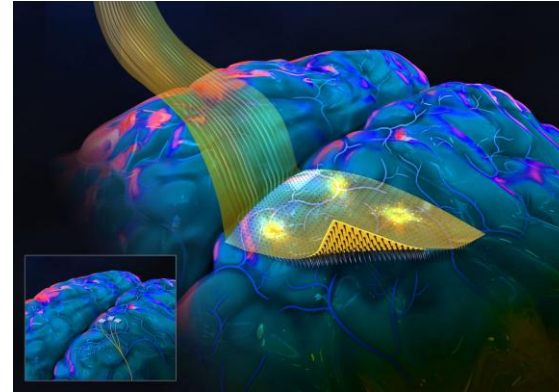
- 2018 – 2022: B.S. in Electrical Engineering, UC San Diego
 - Concentration: machine learning and controls
 - E & M fundamentals; analog & digital circuits; estimation statistics; digital signal processing
 - Research in synthetic data generation for autonomous driving applications
- 2023 – 2025: M.S. in Electrical Engineering, UC San Diego
 - Concentration: systems and circuits
 - Biomedical circuits; RF circuits; VLSI; data networks; 5G transceivers
 - **Hardware and firmware engineer for NIH-funded wireless neuromonitoring project**
- Current occupation: Quartus Engineering
 - Cable harness and PCB design for defense and aerospace opto-mechanical systems
- Pastimes:
 - Oil painting
 - Guitar
 - Fish, spider, and ant keeping

Neuromonitoring Project Goal

- About a third of people with epilepsy have seizures not controllable by medications – often resection or neuromodulation is required
- Intracranially monitor patients using high-resolution electrodes to acquire a better “picture” of the affected regions
 - Record data of unpredictable episodes
 - Clinicians more informed during surgery
- Make it easy to take home and live life as usual

Neural Interface

- Dr. Shadi Dayeh's Integrated Electronics and Biointerfaces Laboratory
 - Ultra high-density, thin-film surface and depth electrodes
 - Patented “platinum nanorod” interface for low impedance



Surface grid

- 4096 recording
- 256 stimulation



Depth probe

- 128 recording
- 16 stimulation



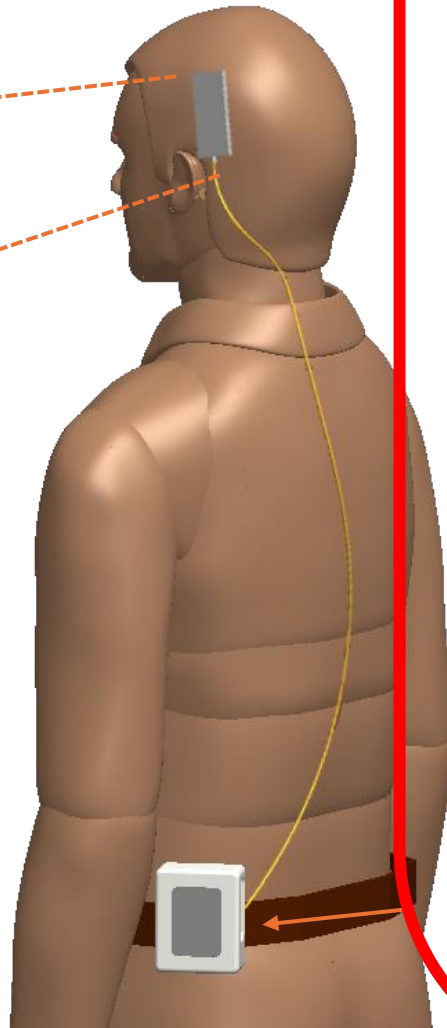
Design Constraints

- 1 surface grid; 8 depth probes
 - Total of 6144 channels, 16-bit depth, 2500 samples/sec
 - At least 210 Mbits/sec of throughput
- Surface grid requires subcutaneous implant
 - Transcutaneous power and data delivery
- Neural signal acquisition and stimulation
 - Multiple off-the-shelf chips
 - Many digital buses running in parallel
- Portable and long-lasting battery
 - Data transmission off person entirely wireless
 - Simple disconnect and recharge
- Easy, intuitive interface to use

Surface System

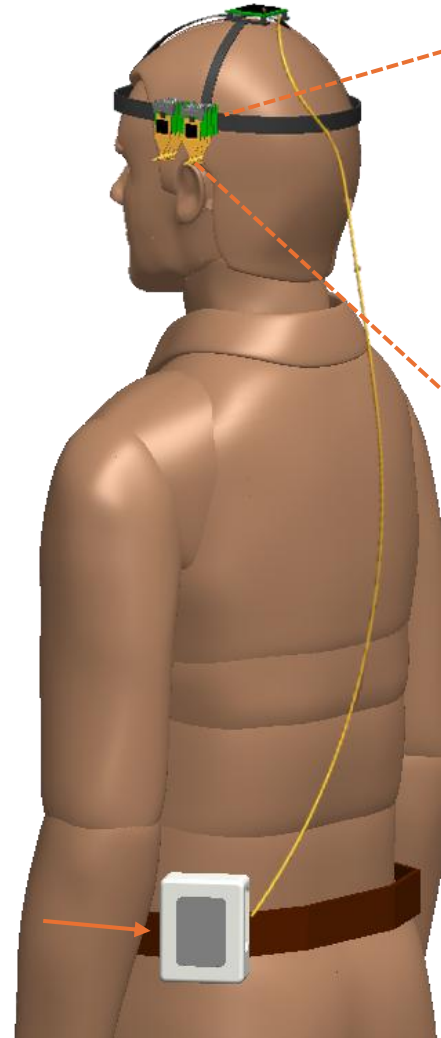


Implanted Unit



Depth System

Processing Unit

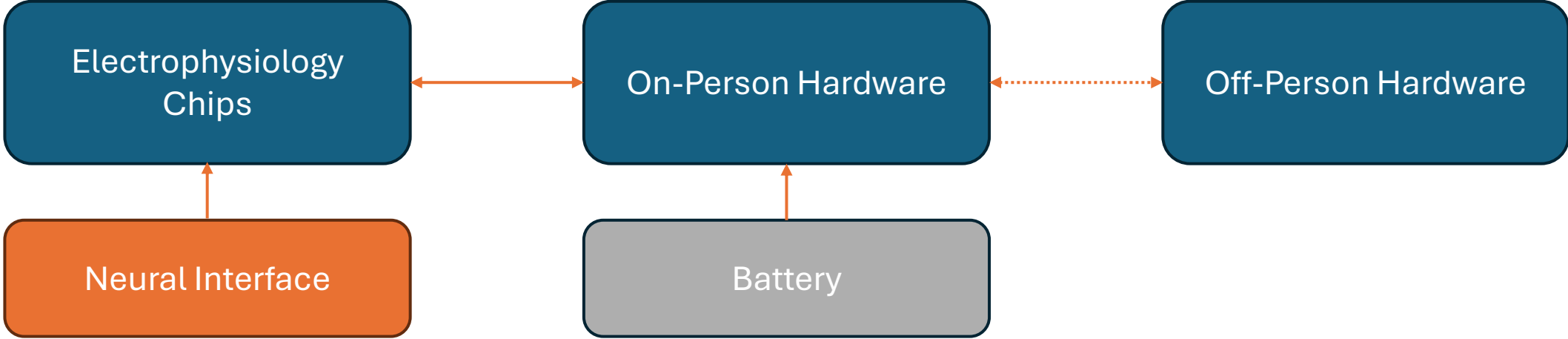


Depth Probe
Headstage

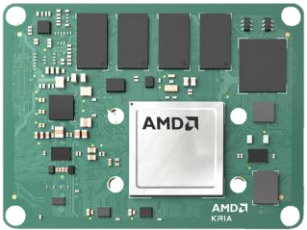


- Design a scalable processing unit and depth system
- Collaborate with surface system engineers
- Obtain long-term data in trails

High-Level Architecture



FPGA + Processors



Wi-Fi



RHS2116 Digital Electrophysiology Stimulator/Amplifier Chip



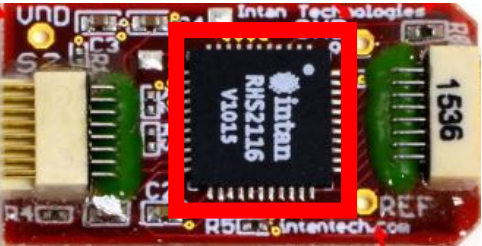
RHS2116

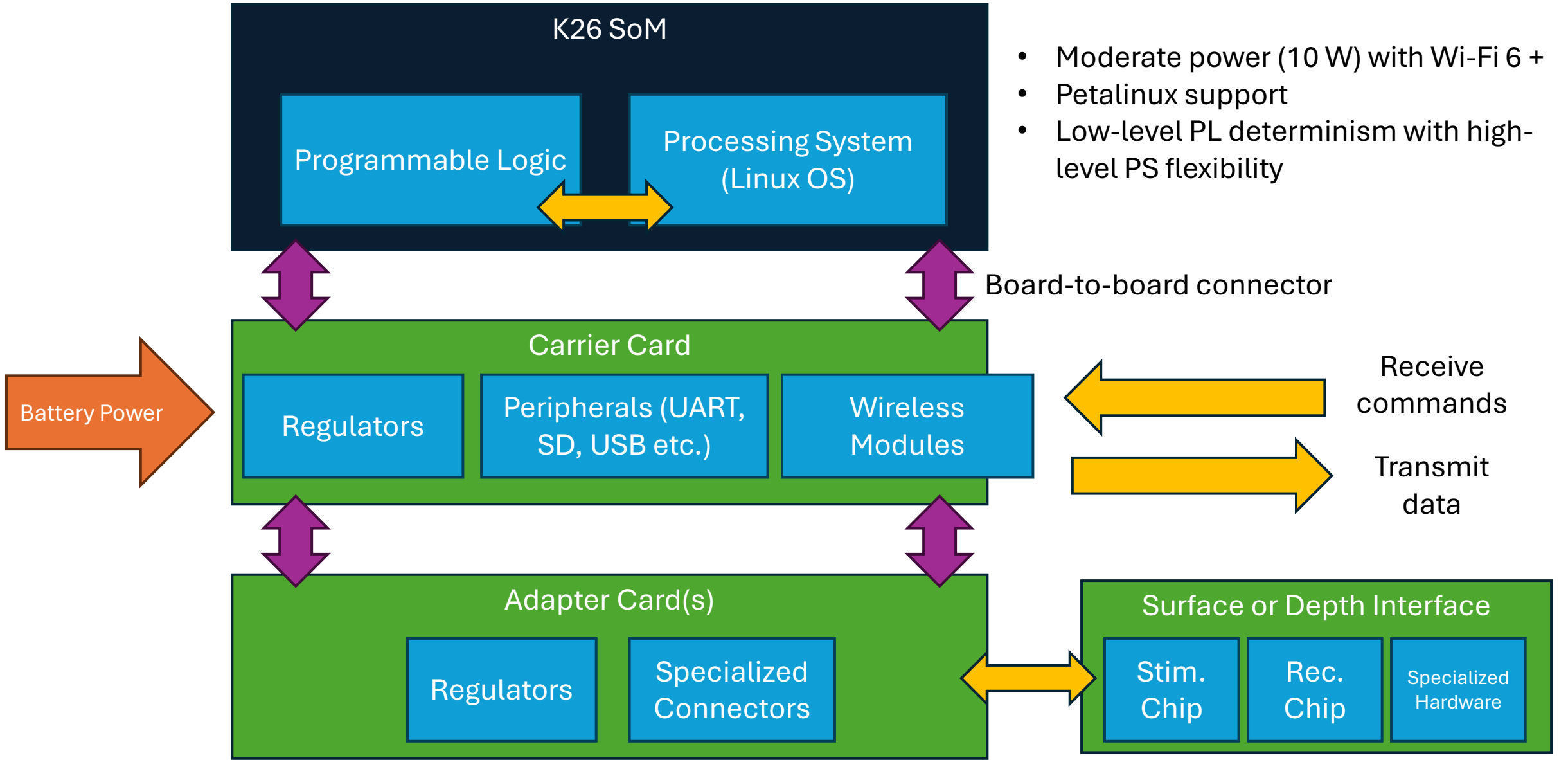
Digital Electrophysiology Stimulator/Amplifier Chip



20 January 2016; updated 13 May 2021

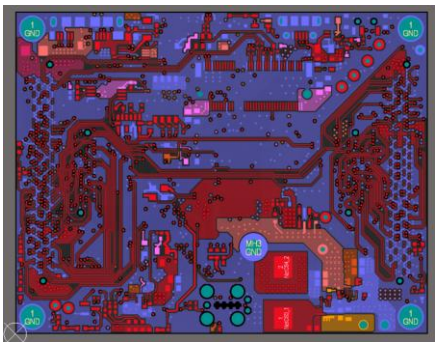
See page 15 for important addendum from May 2021





Carrier Card

- Interfaces with K26 SoM's HD connectors
- Provides to SoM
 - Power regulation and sequencing
 - USB-C PD 2.0 negotiation for beyond 15 W
 - Memory (SD card and EEPROM)
 - Data peripherals (USB 3.0, Wi-Fi 6E)
 - PCIe over M.2
 - Auxiliary functions (UART, JTAG, current monitoring, accelerometer...)
- Extracts from SoM
 - FPGA I/O down to adapter cards over board-to-board connectors
 - Surface and depth signals coexist
- 8-layer controlled impedance



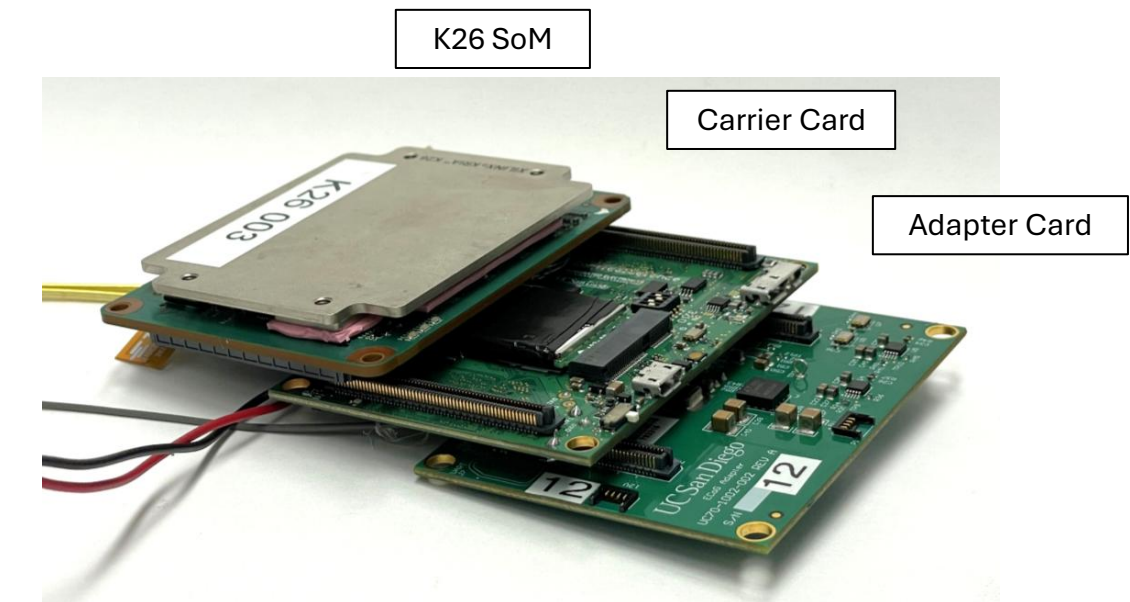
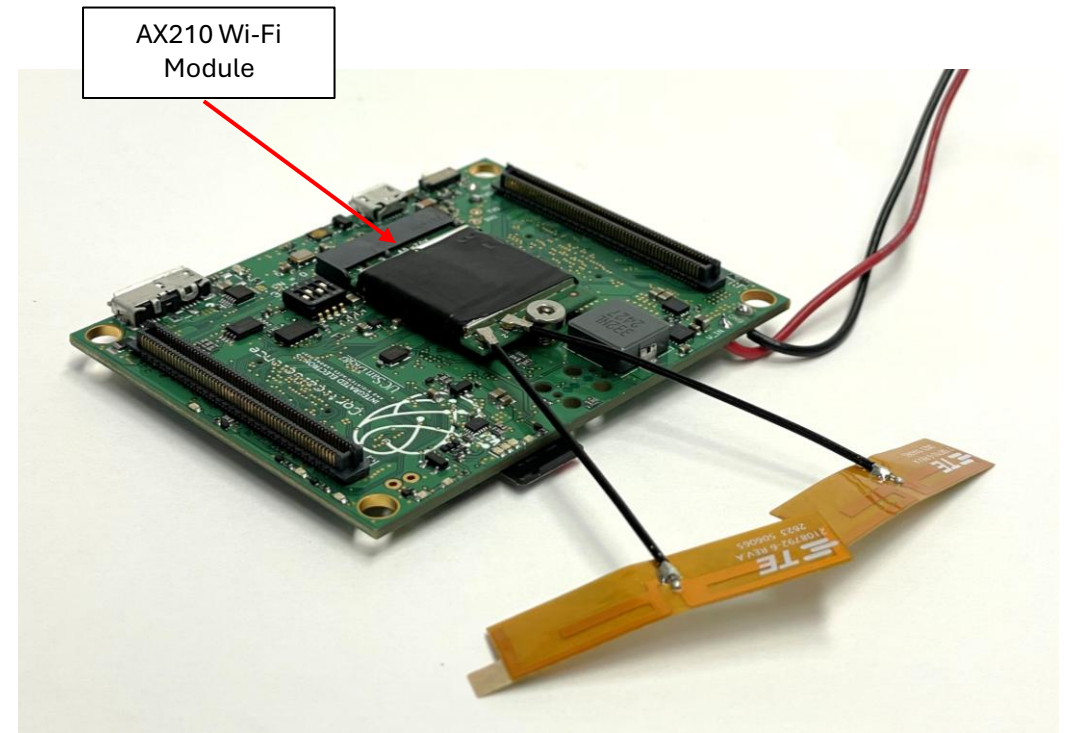
Top



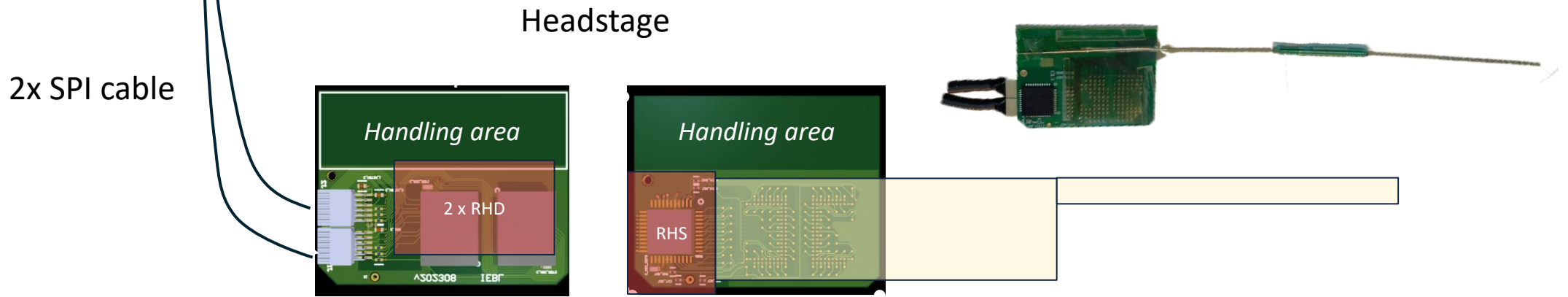
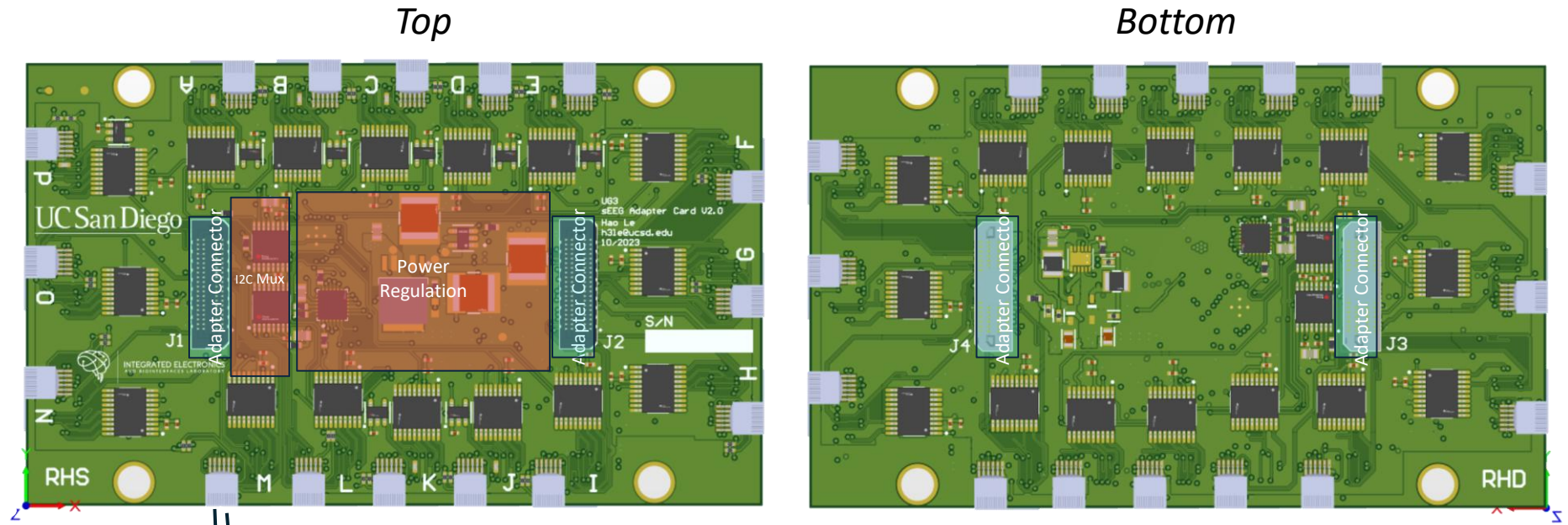
Power



Signal



Depth Adapter Card

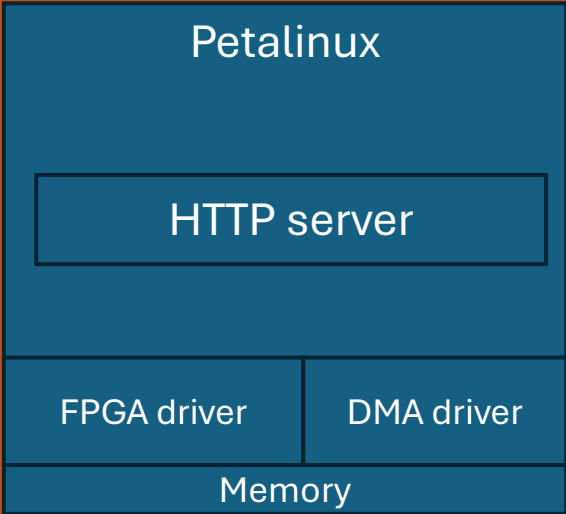


128 recording, 16 stimulation

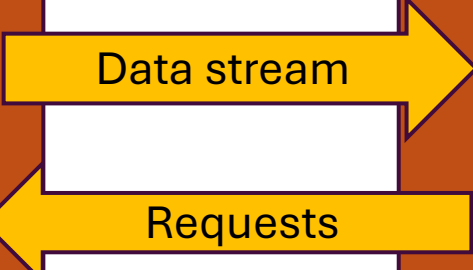
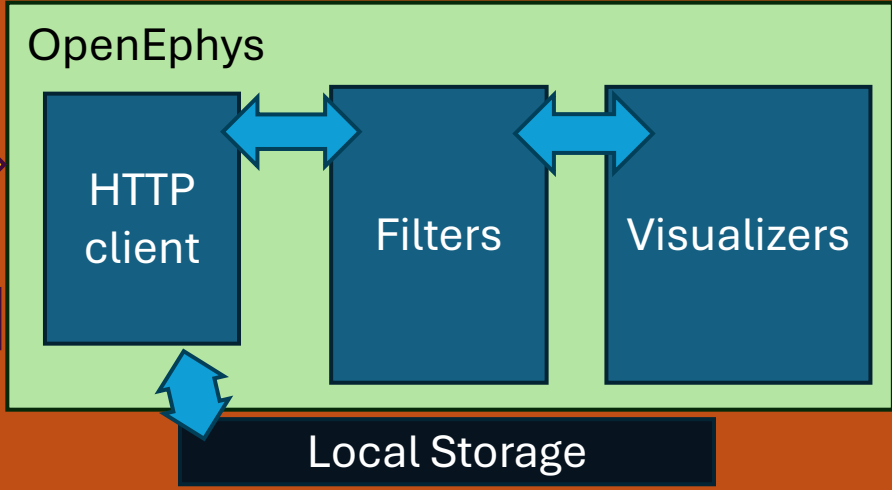
On-Person Hardware

Off-Person Hardware

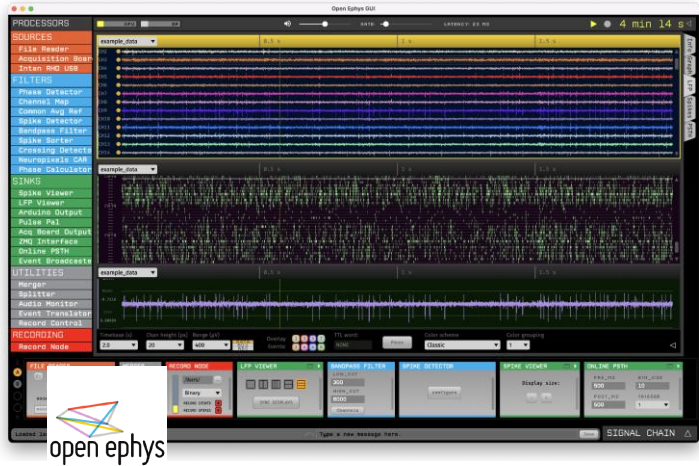
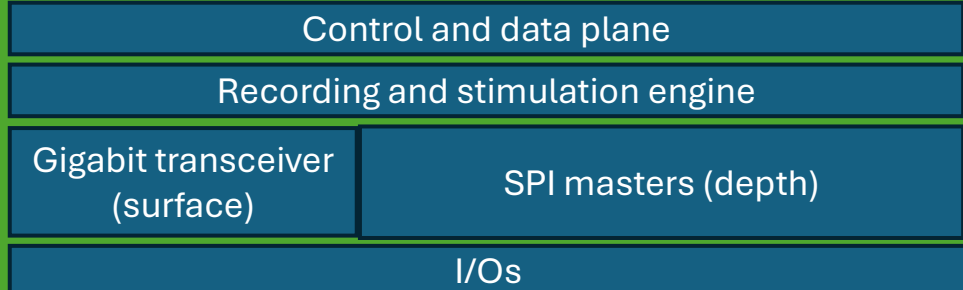
Processing System Domain



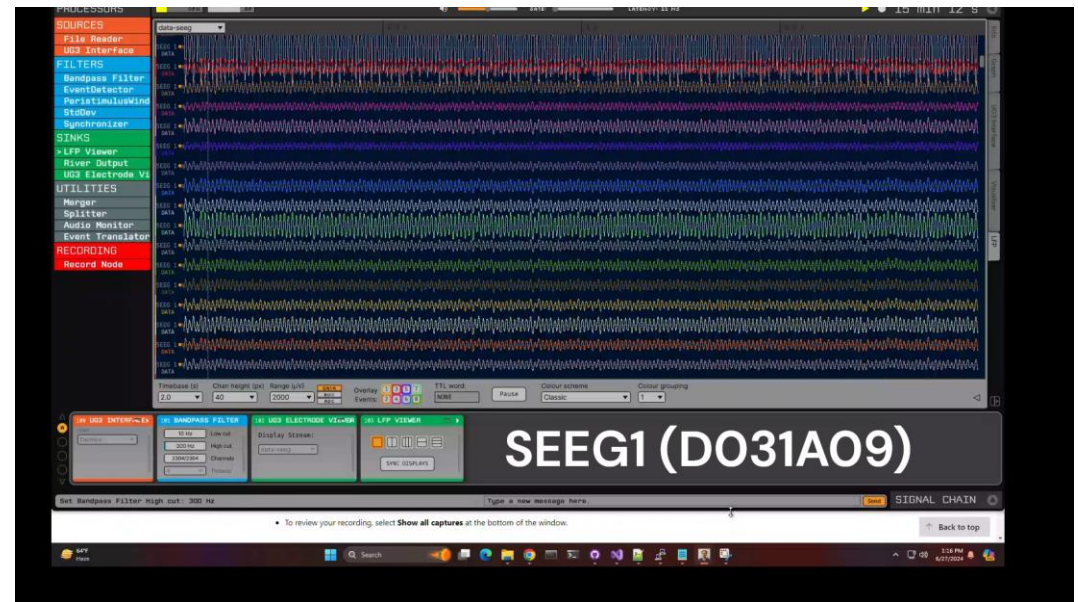
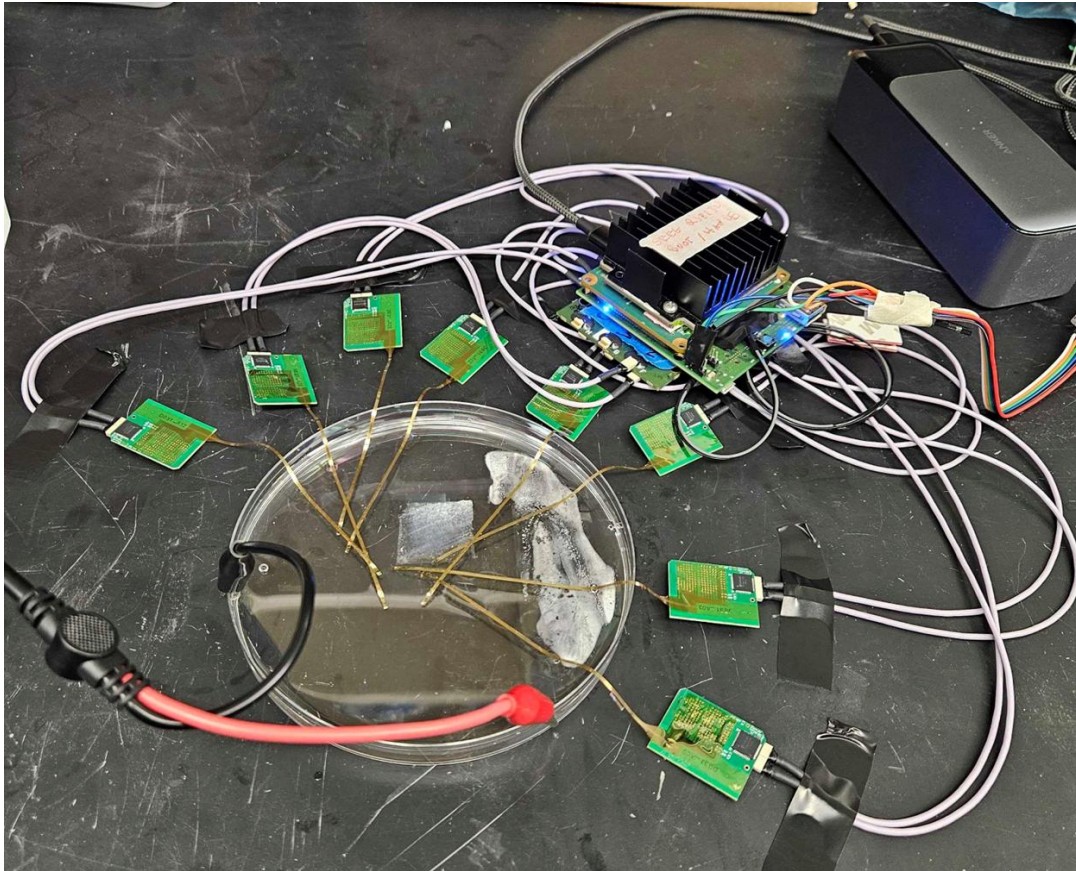
Windows



Programmable Logic Domain

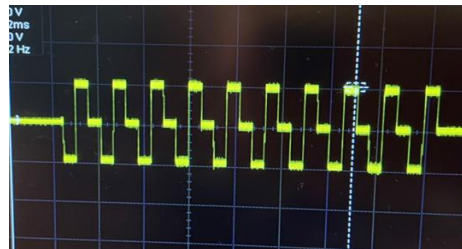


- Open-source GUI platform with community support
- Write backend client code to receive data
- Send data down processing chain to visualize and record
- Custom plugins to further process data

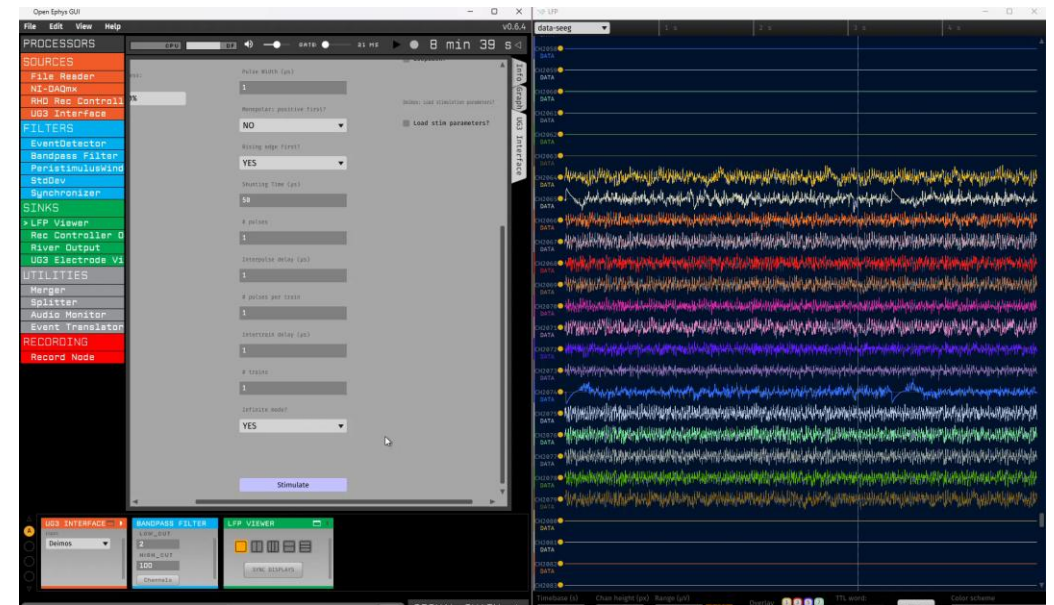


Waveform generator recording validation

- Benchtop validation of 8-depth-probe system
- Recording @ 2.5 kS / s
- 70 us min. stimulation
- OpenEphys as GUI
- Too bulky to wear on head

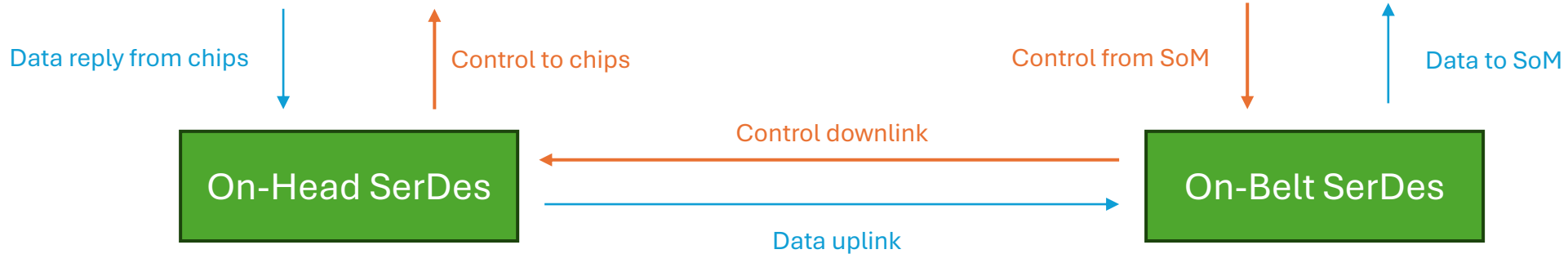
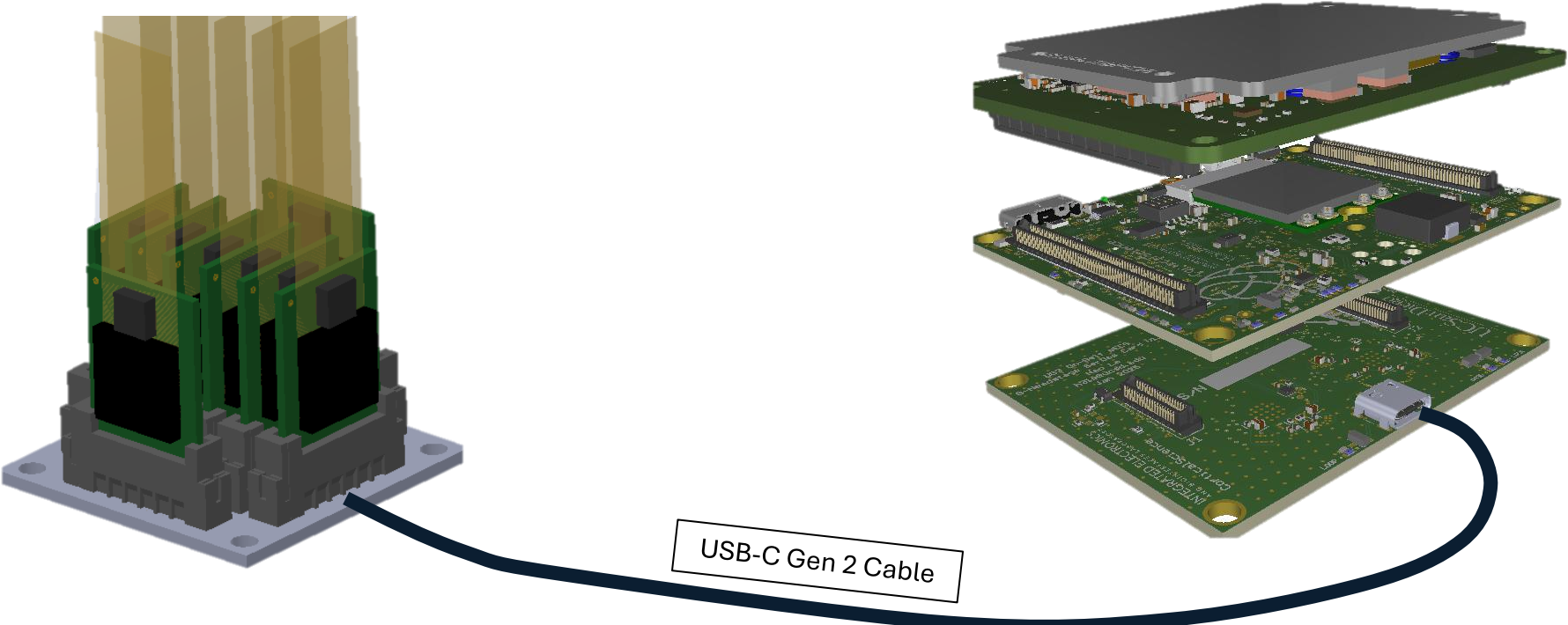


Stimulation train



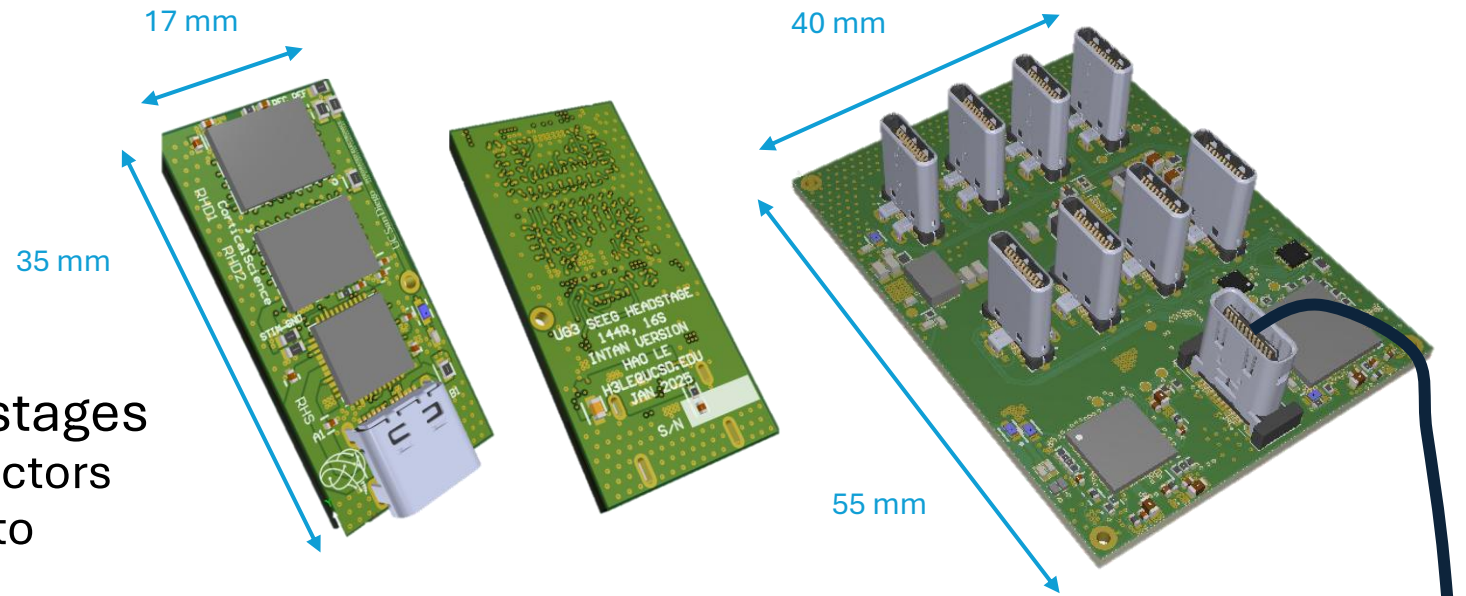
Stimulation GUI example

SerDes Design



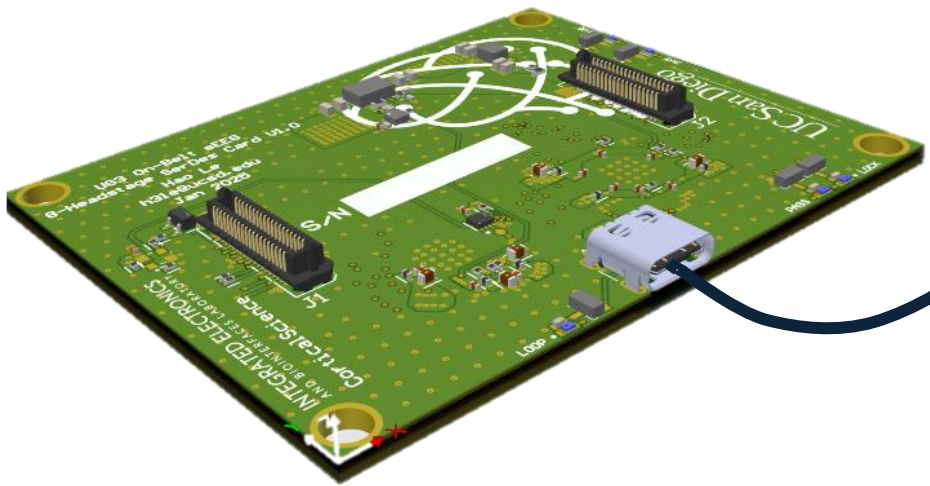
SerDes Design

- Chose USB-C connectors for Headstages
 - Smaller form factor than edge connectors
 - Durable over many use cycles; easy to replace
- SerDes chip pairs from Texas Instruments
 - 75 MHz max I/O clock
 - 2.1 Gbps link rate
 - Able to support all Headstages at 2.5 kS/s
- Single USB-C gen 2 cable chosen as physical link
 - 5 Gbps max link rate
 - (4) standard twisted pairs
 - High current capacity for power delivery

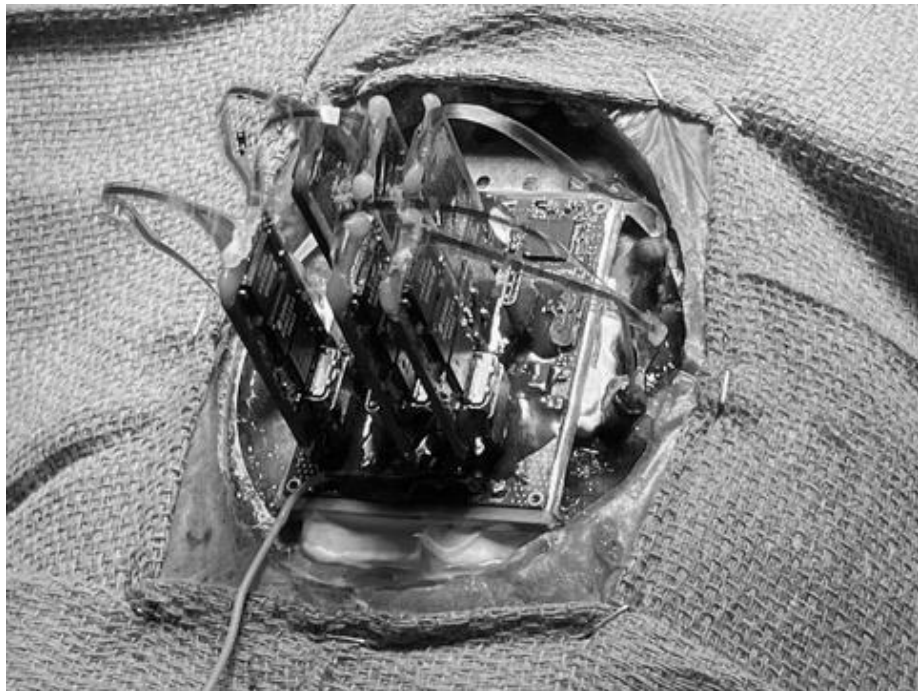
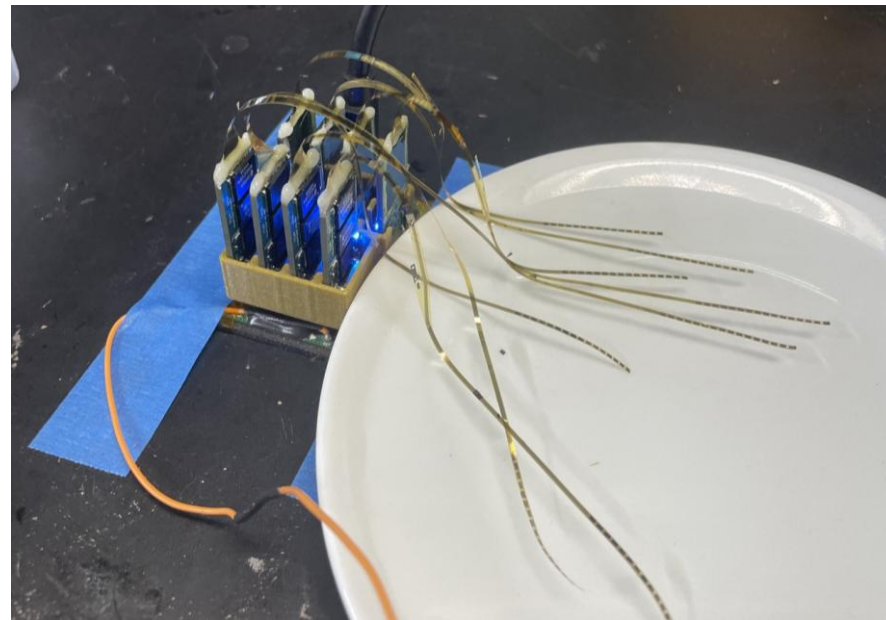
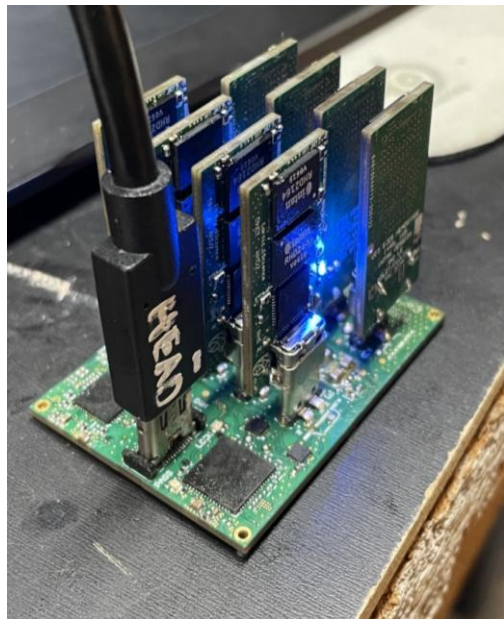


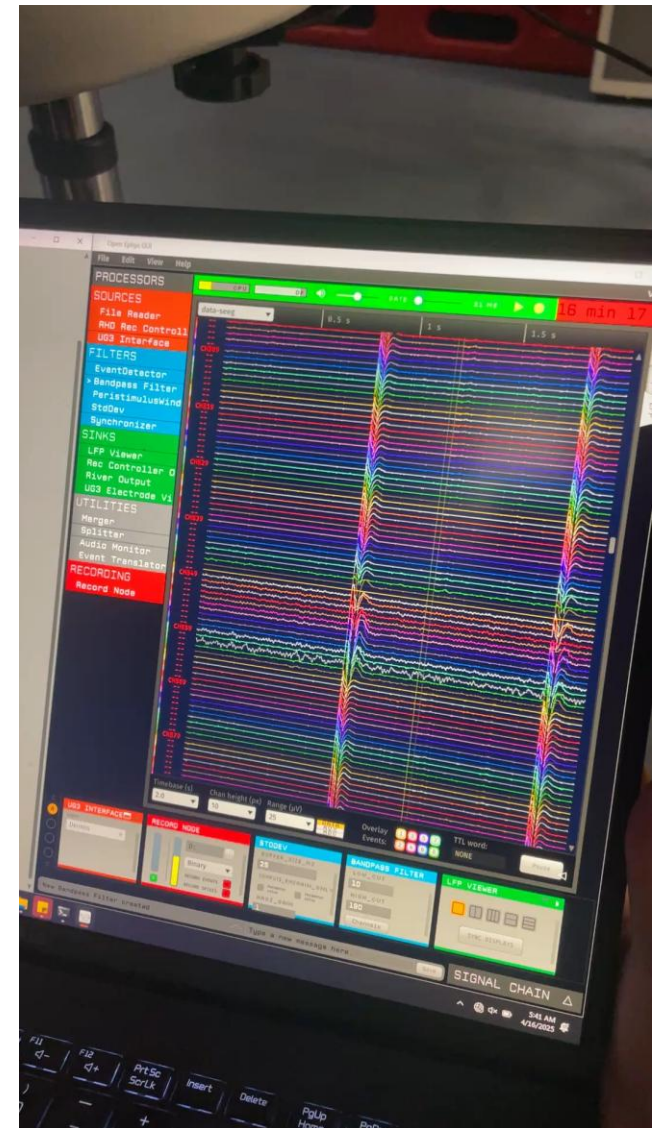
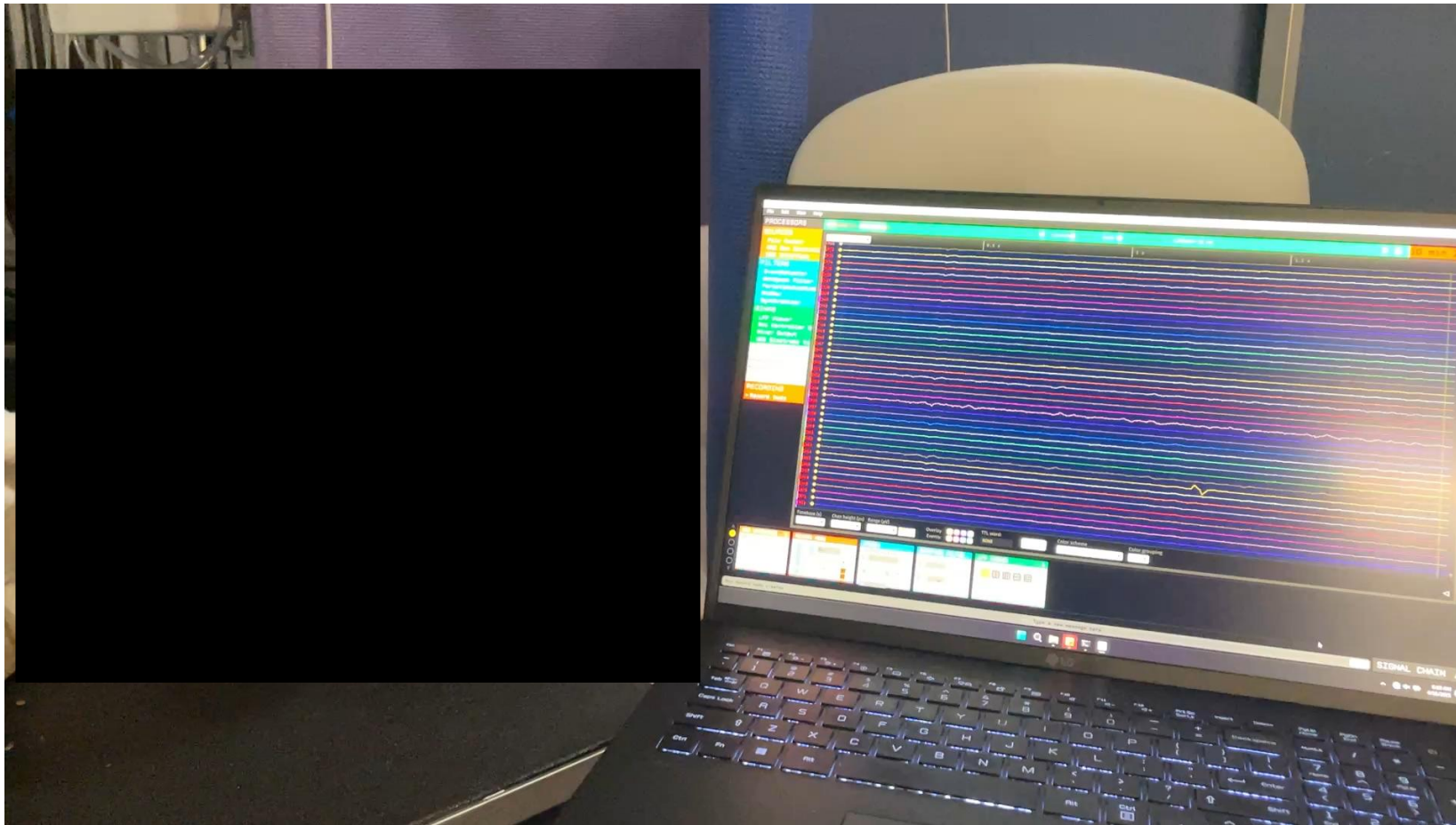
Headstage

On-Head SerDes



On-Belt SerDes

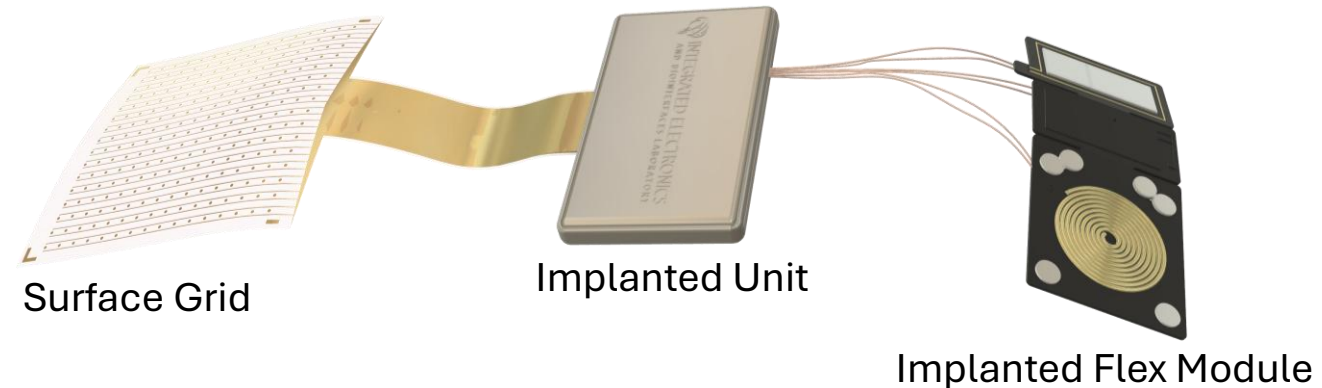


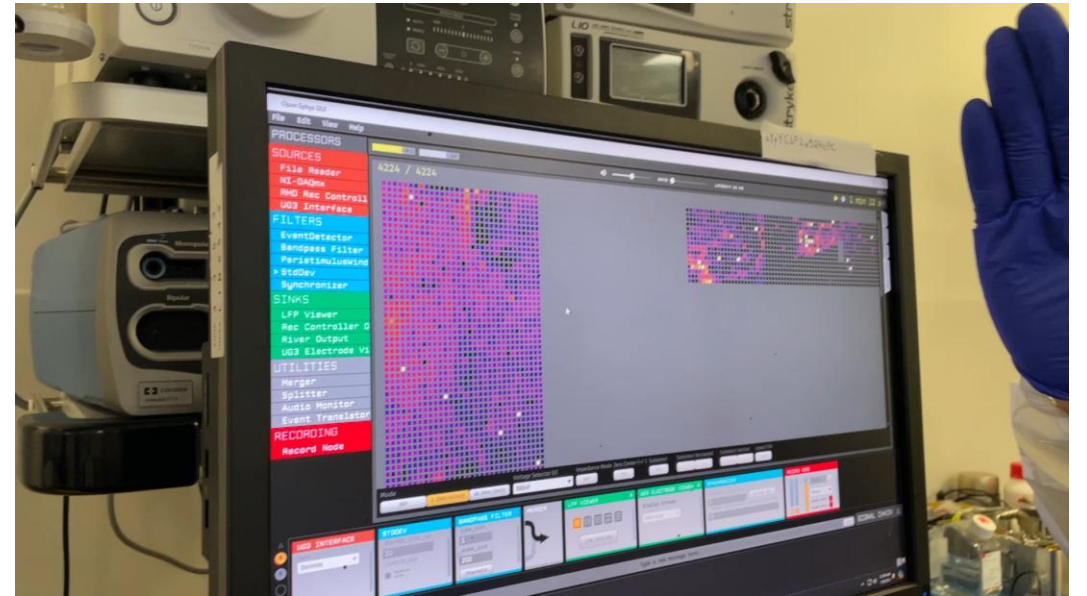
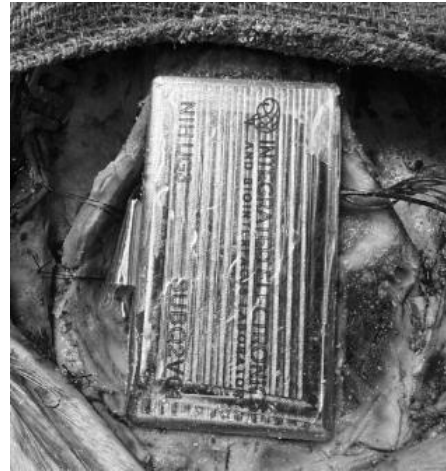


*Real-time monitoring and stimulation
8 hours of continuous data on 20,000 mAh battery*

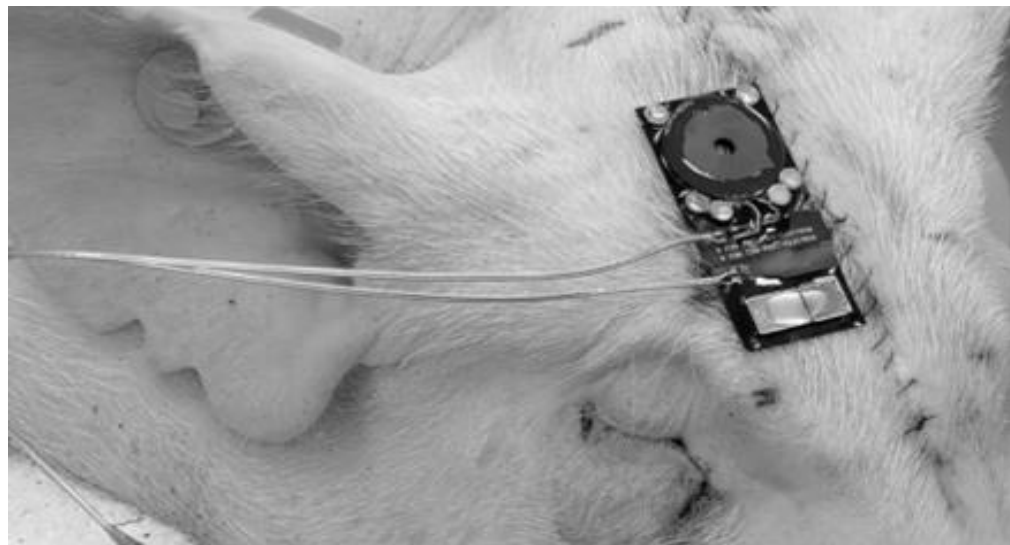
Surface System

- Fully implantable unit containing PolarFire FPGA
- Inductively-coupled transcutaneous links
 - Power downlink
 - Data uplink
- Received data decoded by SoM gigabit transceiver
- Surface adapter card contains
 - BLE module for low-speed control
 - LC tank circuitry for wireless power
 - Twin-axial link to on-head flex module

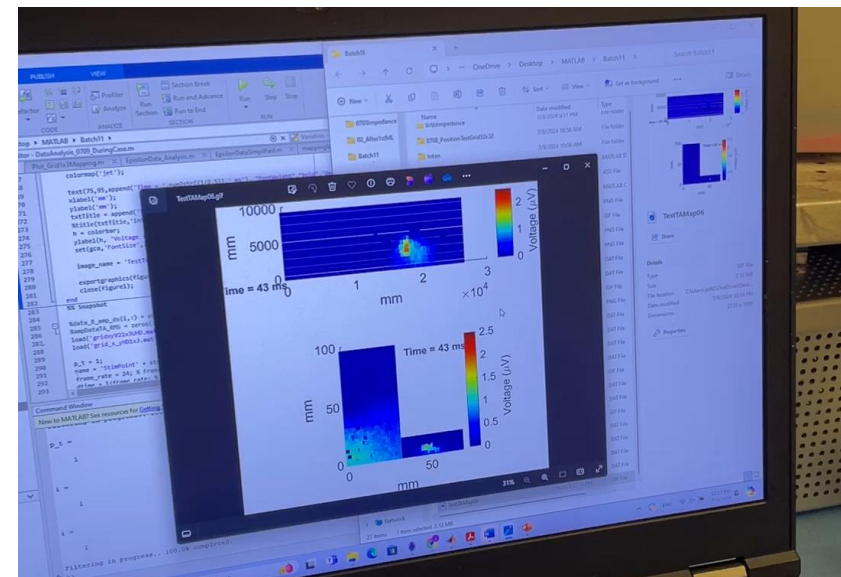




Real-time electrode viewer during grid re-placement



Implant site and external flex module alignment



Stimulation-evoked trial-average potential

Wireless Neuromonitoring System

- Realized a portable, high-channel-count, high-speed, wireless neural data acquisition system
- Central SoM: FPGA + Processing System
- PCBs to enable Wi-Fi connectivity and various peripherals
- Adapting PCBs to enable interface with surface and depth devices
- Crafted downlink control and uplink data pipeline
- Extended open-source GUI platform to control, receive, visualize, and record data stream
- Proved feasibility with several animal cases

